CV of Aryabartta Sahu (www.iitg.ac.in/asahu/)

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Aryabartta Sahu **:** Associate Professor, Department of CSE, IIT Guwahati, Assam-781039
Area of Interest **:** HPC, Cloud System, Multicore System (Architecture, Scheduling and Mapping) and Embedded System
DoB **:** *****1978

Summary of educational qualifications:

- **PhD Comp. Sc. & Engg**. IIT Delhi, Embedded System, Supervisor: M. Balakrishnan and Preeti Rajan Panda, Year of graduation 2009-2010
- **M. Tech. CS** from Utkal University, 2003 with 82% (with HONS)
- M. Sc. Electronics, Sambalpur University, 2000 with University Rank 1, Gold Model, 1st class (75.01%,), **Qualified GATE 2000 and 2001 in Electronics and Communication Engg.**
- **B. Sc. Physics,** Rajendra College Bolangir, Sambalpur University, 1998, 1st class with Distinction
- Both 10^{th} and 12^{th} with 1^{st} class from BSE and CHSE Orissa.

Particulars of present and past employments

- IIT Guwahati, Associate Professor, Teaching & Research, April 2016- Till date
- IIT Guwahati, Assistant Professor, Teaching & Research, December 2009- April 2016

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Publications in Journals

1. Rakesh Pandey, Aryabartta Sahu: Performance and Area Trade-Off of 3D-Stacked DRAM Based Chip Multiprocessor with Hybrid Interconnect. *IEEE Transaction on Emerging Topics of Computing*. 9(4): 1945-1959 (2021) **TETC, IF=7.691**

2. Manoj Kumar, Aryabartta Sahu, Pinaki Mitra: A comparison of different metaheuristics for the quadratic assignment problem in accelerated systems. *Applied Soft Computing*. 100: 106927 (2021), **ASC, IF=6.725**

3. Chinmaya Kumar Swain, Aryabartta Sahu, Reliability Ensured Efficient Scheduling With Replication in Cloud Environment, *IEEE System Journal*, 2021, DOI: 10.1109/JSYST.2021.3112098, 9557876, **SysJour, IF=3.91**

4. Rakesh Pandey, Aryabartta Sahu: Run-time adaptive data page mapping: A Comparison with 3D-stacked DRAM cache. *Journal of System Architecture 1*10: 101798 (2020), **JSA, IF=3.77**

5. Manojit Ghose, Aryabartta Sahu, Sushanta Karmakar: Urgent point aware energy-efficient scheduling of tasks with hard deadline on virtualized cloud system. *Sustain. Computing: Informatics System*, 28: 100416 (2020) **IF=4.028**

6. Manojit Ghose, Sawinder Kaur, Aryabartta Sahu: Scheduling real time tasks in an energy-efficient way using VMs with discrete compute capacities. *Computing* 102(1): 263-294 (2020), **2020 Core Rank A, IF=2.95**

7. Chinmaya Kumar Swain, Ravi Kumar, Aryabartta Sahu: Edge Data Distribution as a Network Steiner Tree Estimation in Edge Computing. *Computing* (2024), **2020 Core Rank A, IF=2.95**

8. Chinmaya Kumar Swain, Aryabartta Sahu: Interference Aware Workload Scheduling for Latency Sensitive Tasks in Cloud Environment. *Computing* 104(4): 925-950 (2022)**. Core Rank A, IF=2.95**

9. Chinmaya Kumar Swain, Neha Saini, Aryabartta Sahu: Reliability aware scheduling of bag of real time tasks in cloud environment. *Computing* 102(2): 451-475 (2020) 2**020 Core Rank A, IF=2.95**

10. Vasudevan Madampu Suryasarman, Santosh Biswas, Aryabartta Sahu: RSBST: an Accelerated Automated Software-Based Self-Test Synthesis for Processor Testing. *J. Electron. Test.: Theory and Application* 35(5): 695-714 (2019) **JETTA, IF=1.01**

11. Vasudevan Madampu Suryasarman, Santosh Biswas, Aryabartta Sahu: Automation of Test Program Synthesis for Processor Post-silicon Validation. J *J. Electron. Test.: Theory and Application* 34(1): 83-103 (2018) , **JETTA, IF=1.01**

12. Vasudevan Madampu Suryasarman, Santosh Biswas, Aryabartta Sahu: Fragmented software-based self-test technique for online intermittent fault detection in processors. *IET Comput. Digit. Tech.* 15(1): 56-76 (2021), **IF=0.818**

13. Chinmaya Kumar Swain, Bhawana Gupta, Aryabartta Sahu: Constraint aware profit maximization scheduling of tasks in heterogeneous datacenters. *Computing* 102(10): 2229-2255 (2020) **2020 Core Rank A, IF=2.95**

14. Tarun K. Agrawal, Aryabartta Sahu, Manojit Ghose, R. Sharma: Scheduling chained multiprocessor tasks onto large multiprocessor system. *Computing* 99(10): 1007-1028 (2017) **2020 Core Rank A, IF=2.95**

15. Manojit Ghose, Aryabartta Sahu, Sushanta Karmakar: Energy Efficient Online Scheduling of Real Time Tasks on Large Multi-threaded Multiprocessor Systems. *J. Inf. Sci. Eng.* 34(6): 1599-1615 (2018), IF=0.541

Publications in Conference

1. Aryabartta Sahu, "Temperature Aware Scheduling and Mapping of Multiphase Application on to Chip Multiprocessor", in *ACM/IEEE/IFIP Design automation and Test in Europe, (DATE 2016)*, March 14-18 2016. **(single author), One of the top conerence in Design Automation Area**

2. Shubhradeep Roy, Suvarthi Sarkar, Aryabartta Sahu, Profit Maximization using Colloborative Storage Management in Multi-tier Cloud System. **IEEE HiPC 2023**

3. Manojit Ghose, Krishna Prabin Pandey, Niyati Chaudhary, Aryabartta Sahu**:** Soft Reliability Aware Scheduling of Real-time Applications on Cloud with MTTF constraints, **Appeared in IEEE/ACM CCGrid 2023.**

4. Aryabartta Sahu, M. Balakrishnan, Preeti Ranjan Panda: A generic platform for estimation of multi-threaded program performance on heterogeneous multiprocessors. DATE 2009: 1018-1023

5. Avadhesh Sharma; Chinmaya Kumar Swain; Aryabartta Sahu: Efficient Welfare Maximization in Fog-Edge Computing Environment; *IEEE HPCC/SmartCity/DSS 2021*, **Core Ranking B Catagory**

6. Chinmaya Kumar Swain; Vaibhav Gupta; Aryabartta Sahu : Energy Efficient and QoS Aware Multi-Level Mobile Cloud Offloading, *IEEE HPCC/SmartCity/DSS 2021*, **Core Ranking B Catagory**

7. Vasudevan Madampu Suryasarman, Santosh Biswas, Aryabartta Sahu: Automated Low-Cost SBST Optimization Techniques for Processor Testing. *IEEE VLSI Design 2021*: 299-304

8. Rakesh Pandey, Aryabartta Sahu: Access-Aware Self-Adaptive Data Mapping onto 3D-Stacked Hybrid DRAM-PCM Based Chip-Multiprocessor. *IEEE HPCC/SmartCity/DSS 2019*: 389-396, , **Core Ranking B Catagory**

9. Vasudevan M. S, Santosh Biswas, Aryabartta Sahu: RSBST: A Rapid Software-Based Self-Test Methodology for Processor Testing. I*EEE VLSI Design 2019*: 112-117

10. Chinmaya Kumar Swain, Aryabartta Sahu: Interference Aware Scheduling of Real Time Tasks in Cloud Environment. *IEEE HPCC/SmartCity/DSS 2018*: 974-979, **Core Ranking B Catagory**

11. Manojit Ghose, Pratyush Verma, Sushanta Karmakar, Aryabartta Sahu: Energy Efficient Scheduling of Scientific Workflows in Cloud Environment. I*EEE HPCC/SmartCity/DSS 2017*: 170-177
12. Sawinder Kaur, Manojit Ghose, Aryabartta Sahu: Energy Efficient Scheduling of Real-Time Tasks in Cloud Environment. *IEEE HPCC/SmartCity/DSS 2017*: 178-185
13. Rakesh Pandey, Aryabartta Sahu: Efficient Mapping of Multi-threaded Applications onto 3D Stacked Chip-Multiprocessor. *IEEE HPCC/SmartCity/DSS 2017*: 324-331
14. Aryabartta Sahu, Saparapu Ramakrishna: Creating heterogeneity at run time by dynamic cache and bandwidth partitioning schemes. ACM SAC 2014: 872-879
15. Saurav Kumar, Aryabartta Sahu: Benchmarking and Analysis of Variations of Work Stealing Scheduler on Clustered System. IEEE PDCAT 2014: 28-35
16. Sahil Kumar, Nitesh Singal, Aryabartta Sahu: Comparison of Binding Approaches of Scheduled Multiphase Application onto Linear Multicore Architecture. IEEE PDCAT 2014: 90-97
17. Bhoopendra Kumar, Aryabartta Sahu: Online Scheduling of Applications on 3D Stacked Large Chip Multiprocessor. IEEE PDCAT 2014: 166-173
18. Manojit Ghose, Aryabartta Sahu, Sushanta Karmakar:Energy Efficient Scheduling of Real Time Tasks on Large Systems. IEEE PDCAT 2016: 99-104
19. Manojit Ghose, Aryabartta Sahu, Sushanta Karmakar: Energy Efficient Scheduling of Real Time Tasks on Large Systems. IEEE PDCAT 2016: 99-104

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PhD Supervison (4 completed and 4 continueing)

1. Manojit Ghose, Thesis titled "*Energy aware online task scheduling on multi-cores and cloud*" Jul 2014 Dec 2018 Joint supervision with S.Karmakar
2. M S Vasudevan, Thesis titled "*Enhancement of SBST Techniques for Detection of Processor Faults*" Nov 2014 June 2020, Joint with S. Biswas
3. Rakesh Pandey, Thesis titled "*Efficient Mapping of Multi-threaded Workloads on to Chip Multiprocessors*", July 2014 July 2020
4. Chinmaya Swain, Thesis titled "*Efficient Task Scheduling on Cloud Environment*" July 2016 July 2021
5. K Chitra, Thesis titled "Design policy of DRAM System in Multicore System", Dec 2020 to till date
6. Suvarthi Sarkar, Thesis titled "Compute and Energy Management in Cloud System Setting", July 2021 to --
7. Shubradeep Roy, Thesis titled "Provisioning and Scheduling Storage in Edge-Cloud Environment" July 2021 to --
8. Vasantha Reddy, Thesis titled "Quality and Reliablity Aware IoT sensing service unsing Edge-Cloud System", Dec 2021 to till date

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Summary of Projects involved from 2011

Sl. No.	Title	Spons Agency	Sponsored Amount	Period		Co-PI	PI or CO-PI;
				From	To		
1	Design and Development of	Meity	1999.9 Lakhs	Apr 23	-Apr 26	A. Sahu and 4 faculty	PI-G Trivedi

	AI/ML Co-Processor and Post Quantum Cryptography Co-Processor					from IIT Guwahati	
2	ANUDAKSH (Anusandhan, Niyojaniyata, Udyamita And Dakshta)	Ministry of Skills	150 Crores	Nov21	--	A. Sahu and 4 faculty from IIT Guwahati	PI: G. Trivedi
3	Intel Center of Excellence on Electronics System Design	Intel India Pvt Ltd	3.5 Crores	Dec 21	Dec-25	A Sahu	PI: G. Trivedi
4	AI enabled advanced aquaponics ecosystem for the self-reliance of SC community in Central and Lower Assam	DST	2.68 Crores	Apr-21	Mar-24	A. Sahu and 4 faculty from IIT Guwahati	PI: G. Trivedi
5	Design and Development of Image Processing Algorithms on GPUs for X-Ray based Imaging System	**BARC**	3.9 Laks	Jul 2015	Aug - 2016	--	PI:A Sahu
6	Task and data mapping on 3D stacked memory large chip multiprocessor (LCMP).	IITG	4.8 Lakhs	Aug 2010	Jul-2013	--	PI:A Sahu

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Others Details

Laboratory Set up at IIT Guwaahti

- Modernize Hardware Laboratory with **Xilinx FPGA** (Spartan 6 and Artix7).
- Setup**Intel Xeon Phi** for OpenMP, MPI, and Cilk program acceleration
- Setup **GPU cluster** using two GTX 690 GPU, one GTX 980Ti, one AMD Radeon 270x. Many people of our institute used the setup GPU cluster.
- Involved in department compute server setup and procurement

Teaching Material Development at IIT Guwaahti

- Helped in designing course structure for CS101, CS221, CS223, CS222, CS431 and CS527. Also actively involved in B Tech/M Tech curriculum improvement in 2010, 2017
- Developed a new elective course on High-Performance Computing (**HPC**). I have floated the same course four times
- Act as Reviewer for the curriculum of six-nine months certificate program of E&ICT Academic, IIT Guwahati

Departmental level Admin Activity

- Convenor, Department PG Admission Committee, from 2019-Till date
- DPPC Committee Member Sep-2010 to Mar-2013
- Dept Laboratory In-charge (Sep-2011 to 2015 July)
- Invigilation Duty allocation for MID Sem and End Sem (Sep-2010 to Mar-2013)
- TA Duty Allocation (Sep-2010 to Mar-2013)
- Compute server procurement committee.

- Managing CAES Group Website

Awards / Honours etc.

- IEEE Senior Member
- Gold Medal for securing 1st position in M Sc Electronics at Sambalpur University

Short-term courses / workshops / conferences organized

- Eighth International Conference on Information Systems Security (ICISS 2012), IIT Guwahati, India ICISS 2012 (Role as Publicity Chair)
- Nvidia HPC Workshop (One of the Organizer) 2014
- Xilinx Workshop (One of the Organizer and Associate person) 2014
- Computer Architecture lecture series and workshop at IIITDM Jabalpur 2012
- Intel Xeon Phi High-Performance Workshop (one of the organizers cum speaker) Aug 2015
- **Served as Finance Chair and Publication Chair and co-hosted online** of VLSI Design 2021
- Intel FPGA Faculty Development Program 20-21, 27-28 Nov 2020
- VDAT (Website Chair) May 2016

Course Taught

- CS528 High-Perf.Computing, UG/PG, Single, Strength (4, 43, 260,183) taught four times
- CS523 Adv. Comp. Architecture, PG, Single Strength 20, taught once
- CS223 Hardware Laboratory, UG, Single 80, Taught six times
- CS221 Digital Design UG Single (1) + Shared (4) Strength 140, taught 5 times
- CS101 Introduction to Computing, UG, Shared, Strength 800, taught three times
- CS222 Comp. Org. & Architecture UG Single + Shared Strength 80, 140, taught two times
- CS421 Comp. Peripherals &Interface UG Single Strenght 60 taught once
- CS341 Operating System UG Single, Strength 200, Taught twice
- CS594: Python Programming Lab, PG, Single 20, taught once
- CS431 Programming Language Lab UG, Single 80 taught twice
- CS110 Computing Laboratory UG Shared mode, 800, taught twice