DEPARTMENT OF CSE, IIT GUWAHATI

Indian Institute of Technology Guwahati (IITG), the sixth member of the IIT fraternity, was established in 1994. IIT Guwahati has been able to build up world class infrastructure for carrying out advanced research and has been equipped with state-of-the-art scientific and engineering instruments. IITG campus is on a sprawling 285 hectares plot of land on the north bank of the river Brahmaputra around 20 kms from the heart of the city. With the majestic Brahmaputra on one side, and with hills and vast open spaces on others, the campus provides an ideal setting for learning.
http://www.iitg.ac.in/

The Department of Computer Science and Engineering, IITG started its academic programme in the year 1995 and provides an outstanding research environment complemented by excellence in teaching. The department offers B.Tech., M.Tech., Ph.D. and Dual (M.Tech.+ Ph.D.) degree programs. The department has a comprehensive curriculum on topics related to all aspects of computer hardware and software with an emphasis on practical learning. The department has around 30 faculty members actively involved in various cutting edge research domains in CSE.
http://www.iitg.ac.in/cse/

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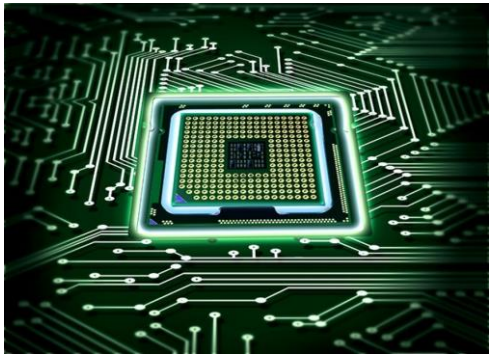
ABOUT TEQIP-III

TEQIP an initiative of MHRD, Government of India is a long term program for quality enhancement and resource sharing of technical institutions in India. TEQIP-III was started in 2017-18 as Central Sector Scheme with a special focus on the low income states, north-eastern states, hill states and islands. KIT (Knowledge Incubation Cell for TEQIP), established at IIT Guwahati under 2nd phase of TEQIP, functions as a multi-disciplinary as well as interdisciplinary Innovation Incubation Centre with a focus to impart knowledge, infusing innovation and leading a path to achieve academic excellence. http://www.iitg.ac.in/cet/teqip3.html

TEQIP-III SPONSORED SHORT TERM COURSE ON C-BASED VLSI DESIGN: SYNTHESIS, OPTIMIZATION AND VERIFICATION



1st - 5th April, 2019

Organised by

Department of Computer Science and Engineering,

In collaboration with

KIT-Centre for Educational Technology
IIT Guwahati

ABOUT THE COURSE

C-Based VLSI Design or High-level Synthesis (HLS) tools made significant progress in the past few years, improving the design productivity for hardware accelerators. C-Based VLSI design is becoming mainstream in electronic Design Automation (EDA) industries to create specialized system-on-chip (SoC) architectures. The researchers have proposed various strategies for scheduling, allocation and binding and data path and controller design, explored the impact of compiler optimizations of HLS synthesis results, suggested various optimization strategies for better area, power and timing results of generated circuits. However, areas like HLS for FPGA targets, HLS for secure and reliable hardware, impact of C-coding style on final RTL have not been explored yet properly. Particularly, the verification of HLS is not explored yet properly. The objective of this course is to provide a comprehensive overview of synthesis, optimization and verification technologies of existing C-based VSLI design. Moreover, the current research trends in C-based VLSI will be discussed. This course will help the participants to understand (i) the overall C-based VLSI flow, (ii) How a C-code will be converted to its equivalent hardware, (iii) How to write C-code for efficient hardware generation, (iv) How the common compiler optimizations can help to improve the circuit performance, (v) HLS for security and reliability of hardware, (vi) HLS for FPGA targets, (vii) Optimizations at RTL level and (viii) Verification challenges of HLS.

COURSE PLAN

Day 1: Introduction to Electronic Design Automation, Introduction to C-Based VLSI Design (High-level Synthesis (HLS)), Scheduling Techniques

Day 2: Resource allocation and binding, Compiler optimization in HLS, HLS for FPGAs, Lab session on HLS

Day 3: HLS for security, Fault-tolerant HLS, C coding style for HLS, Lab session on HLS

Day 4: HLS Verification, Recent Trends in HLS, Lab session on HLS Verification

Day 5: RTL optimization Techniques, Effective Teaching Pedagogies.

ELIGIBILTY, REGISTRATION AND SELECTION

The course is open to faculty members of TEQIP mapped institutions. Please refer "Institution List" link of NPIU website http://www.npiu.nic.in/index.htm for list of TEQIP mapped institutions. However, PhD scholars/PG students from these institutions may be accommodated subject to vacancy of seats.

There will be a refundable registration fee of 2500 INR for the participants from TEQIP mapped institutions. Seats that remain unfilled will be open to faculty/students of other institutions with a non-refundable registration fee of 2500 INR. There will be a total of 40 seats for the course based on application followed by short listing.

BOARDING AND LODGING

For participants from TEQIP mapped institutions, based on requests from the applicants, accommodation can be arranged free of cost either in the guest house or student hostels inside IITG campus or in hotels at Guwahati city. Participants from non-TEQIP institutes should make their own arrangements for boarding and lodging. Registration fee will cover course materials and working lunch.

HOW TO APPLY

Interested candidates can find application form, registration details and guidelines in the course webpage link given below http://www.iitg.ac.in/ckarfa/TEQIP3_HLS/teqip3.html

Duly filled application form, endorsement form (approved by the respective head of the institute) and the registration fee Demand Draft (drawn in favour of "**Registrar, IIT Guwahati**", payable at Guwahati) should be sent to **Dr. Chandan Karfa** via speed post to the address mentioned below. Last date for receipt of application form and registration fee DD is **8.3.2019 (Friday).**

The registration fee is refundable subject to participation in the course. Registration fee will not be refunded if the candidate fails to attend the course. Candidates from TEQIP mapped institutions can claim TA & DA from their respective institutions.

Course Coordinator

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Accommodation and Registration Support

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